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Pin-Fin Heatsink Active Antenna Array With Joint Bandwidth Improvement, Footprint Miniaturization and Cooling Benefits

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Abstract
This paper presents a novel heatsink antenna array architecture that addresses electromagnetic (EM) performance, antenna miniaturization, and thermal management challenges in antenna-on-substrate (AoS) configurations. By integrating tilted fin heatsinks onto rectangular patch antennas, the proposed unit element improves convective cooling while maintaining desirable radiation characteristics. A parametric analysis demonstrates that optimizing the fin tilt angle results in an $8\,\%$ reduction in the resonant frequency, effectively miniaturizing the antenna. To further enhance array performance, complementary split ring resonator (CSRR) walls are introduced between elements. These structures significantly reduce mutual coupling (from approximately $-9\,\mathrm{dB}$ to $-15\,\mathrm{dB}$) and more than double the impedance bandwidth, increasing it from $3.3\,\%$ to $7.5\,\%$. The results confirm improved radiation performance with a $12.7\,\%$ operational radiation pattern bandwidth centered at $24\,\mathrm{GHz}$ and stable gain across scan angles. On the thermal side, distributed chip placement and enhanced convective paths reduce chip temperatures from $97.3\,^{\circ}\mathrm{C}$ to $70.3\,^{\circ}\mathrm{C}$ for $1\,\mathrm{W}$ heat power per chip, and from $171.7\,^{\circ}\mathrm{C}$ to $138.9\,^{\circ}\mathrm{C}$ for $2\,\mathrm{W}$ heat power per chip under forced airflow conditions compared to the standard patch array. The proposed dual-functional design provides an efficient and compact solution for future high-power and thermally constrained antenna systems, with promising applications in 5G, radar, and mm-wave communication.

Key terms
Active Antenna; Bandwidth Enhancement; Complementary Split Ring Resonator; Cooling; Phased Array.

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1. Introduction

In active antennas and phased arrays, high-power generating radio-frequency (RF) circuits are integrated with the electromagnetic (EM) radiators [1]. The level of integration depends on the frequency of operation, which can lead to antenna-on-substrate, antenna-in-package or antenna-on-chip concepts [2]. The antenna-on-substrate (AoS) array designs are mostly preferred at low mm-wave bands (Ku-, Ka-bands) in planar substrate stack-ups with patch antennas on one side, and CMOS-based flip-chip implementation on the other side of the substrate [3]. Such arrays are proposed for various wireless communication and sensing applications [4, 5, 6, 7].

One of the key challenges in active antennas is the thermal management. The limited efficiency of the electronics, mainly the power amplifiers (PAs), may cause extreme heat densities and chip temperatures [8]. In the state-of-the-art antenna systems, power-hungry and bulky external coolers, such as fans, heat pipes, and pumped liquids, are utilized on the chip side [9]. These single-sided thermal management solutions have limited cooling capacity as the cooling efficiency drops while moving away from the heat source [10]. Therefore, creating alternative short (i.e. low thermal-resistance) cooling paths in AoS arrays is crucial.

The patch antennas in AoS arrays are in the close proximity of the chips and they are interfacing the surrounding air. This gives the potential for cooling through convection once the heat is conducted from the chip to the antennas (e.g. by thermally connecting the chip to the antenna ground plane and by shorting the patches). However, the standard patches with small metal thicknesses do not have enough surface area and air flow to enhance cooling. An intriguing solution to this problem is

to attach a heatsink (e.g. with cylindrical fins) on top of the patches, which leads to the concept of heatsink antenna [11]. As the heatsink modifies the EM behavior (i.e. matching, radiation pattern) of the standard patches, it becomes challenging to achieve EM-thermal dual-functionality. On the other hand, the extra design degrees-of-freedom in fin dimensions, positions and angles provide a wide search space to optimize the dual performance trade-offs, and even to have some control on the EM performance for customized requirements.

Inspired by the earlier work on finned heatsink antennas [12, 13], the authors proposed a frequency-adjustable heatsink antenna element concept in [14] where the operating frequency is controlled by the fin angles of the heatsinks for fixed patch dimensions. Later in [15] in EuCAP 2025, the authors studied the effect of mutual coupling and its mitigation via complementary split ring resonator (CSRR) walls [16] in an array environment for vertical fins. This paper is a novel extension of these two recent papers, with the goal of miniaturizing the array's footprint by utilizing tilted heatsink fins at the unit element, while enhancing the bandwidth and port isolation by utilizing the CSRR walls at the array level.

The rest of the paper is organized as follows. Section 2 describes the proposed heatsink antenna element, and presents its EM-thermal simulation results. Section 3 explains the major EM issues when such elements are used in an array environment, and proposes thermally-enhanced design solutions to overcome these challenges. Section 4 provides the final EM-thermal simulation results of an 8-element heatsink antenna array for concept demonstration purposes. Section 5 concludes the paper.

2. Proposed Heatsink Antenna Unit Element

The concept of heat-dissipating antennas can be realized by utilizing and modifying different antenna types, such as fully metallic antennas, wire-type antennas, and printed-type antennas. In this study, we will focus on printed antennas, especially rectangular patch designs, because of practical interest and easy integration with electronics. The heat generated by PA can easily be transformed to the patch surface thanks to the thin and layered structure of the PCB. The metallic surface of the patch dissipates the heat by convection; however, the convection surface is limited. To increase the convection surface, we place a heatsink (HS) on top of the patch. Thus, the HS-Antenna consists of a patch and a finned HS structure combined with a very thin thermal glue layer. As the thermal glue layer is very thin, the surface currents that occur in the patch are induced on the HS base and affect radiation. This design aims to improve heat dissipation and the radiation characteristics of the antenna compared to a patch without HS. The unit element (HS-antenna) is designed to provide both electromagnetic and thermal benefits compared to a conventional rectangular patch, which is discussed in the following sections.

2.1. Electromagnetic Model and Results

The electromagnetic part of the antenna element starts with the investigation of the miniaturization capabilities of the HS antenna element. The unit element of this study is created by combining a rectangular patch with a heatsink that has flared

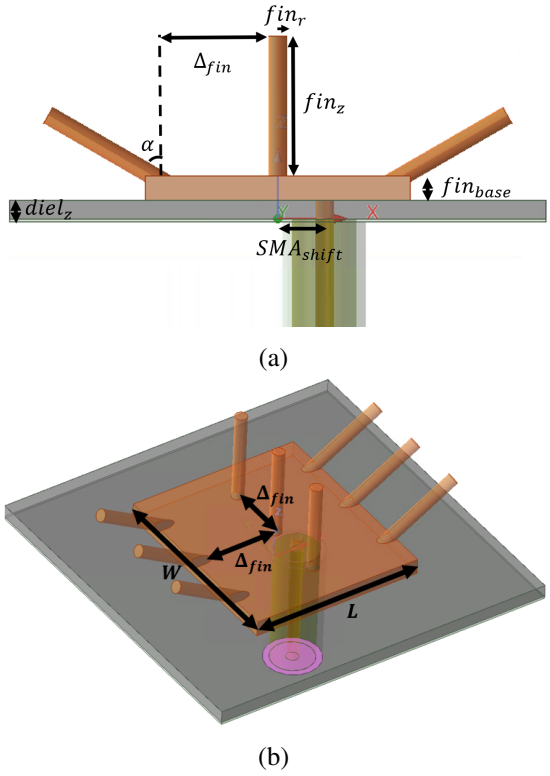


Figure 1: View of the unit element: (a) side, (b) isometric.

fins at the edges. Flaring of the HS fins is aligned to coincide with the radiating edges of the patch to increase the degree of freedom in design, as seen in Fig. 1. The antenna is designed to operate at 24 GHz center frequency. The center frequency of the antenna illustrates a slight change towards lower frequencies within the array structure; therefore, the unit element is arranged to work at 24.2 GHz.

Antenna is numerically modeled with the ANSYS HFSS solver. We analyzed the antenna by first matching its impedance to 50 Ω by arranging the SMA_{shift} variable. Then, a parametric analysis is done on the fin angle α to understand the amount of miniaturization due to the flaring of the fins. The flared HS element affects the impedance matching, providing a frequency shift in the resonance point. The flaring angle miniaturizes the antenna by lowering the operating frequency. The reflection coefficient values of this parametric study can be seen in Fig. 2.

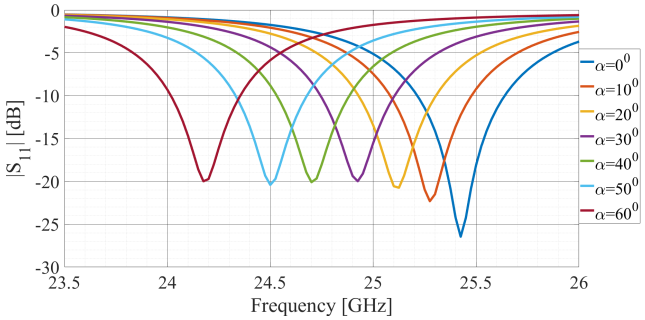


Figure 2: $|S_{11}|$ values of unit element with different α values.

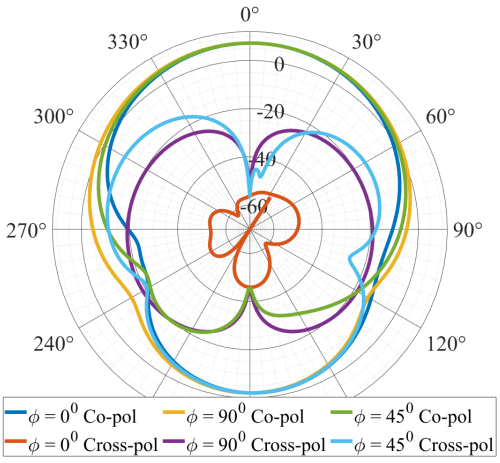


Figure 3: Realized gain co- and cross- polarization polar plots of the proposed HS element.

Table 1: Dimensions of the unit element

Variable	Dimension	Variable	Dimension
fin_r	0.1 mm	SMA_{shift}	0.4 mm
fin_z	1.5 mm	$diel_z$	0.203 mm
fin_{base}	0.2 mm	W	3.3 mm
Δ_{fin}	1 mm	L	2.86 mm
α	60^0	Unit element	5.77 mm

Parametric study on fin angle suggests that the more tilted fins become, antenna resonates in the lower frequencies. Frequency shifting happens as the current path induced on HS increases. The standard rectangular patch antenna resonates at 24.2 GHz with a length (L) of 3.1 mm. This length is now reduced to 2.86 mm. We will use $\alpha = 60°$ design to miniaturize the antenna footprint to its 92 % as compared to the one without the HS. The proposed dimensions of the antenna element can be found in Table. 1. The radiation pattern of the HS antenna is aimed to be a broadside with low cross-polarization. The radiation pattern is obtained with a maximum realized gain of 7.18 dB and cross polarization lower than 45 dB in the broadside direction. Co and cross polarization patterns of the single antenna can be seen in Fig.3 for $\phi = 0°$, $\phi = 45°$, and $\phi = 90°$ angles. The impedance bandwidth ($|S_{11}| < -10$ dB) of the antenna is reduced from 420 MHz to 380 MHz with the introduction of the heatsink structure on top of the patch. However, the HS antenna illustrates exceptional gain improvement in the element scale. The realized gain of the antenna is increased from 6.45 dB to 7.18 dB with the addition of the HS.

2.2. Thermal Model and Results

To assess the thermal performance of the antenna, thermal simulations are needed. The thermal simulations are realized with a CFD solver (ANSYS ICEPAK). The RF chip is modeled as a two-resistor network, where the resistance values are 10 K W^{-1} and 14 K W^{-1} between junction-to-case and junction-to-board [9]. The side view of the ICEPAK setup can be seen in Fig. 4.

The RF chip temperature mainly depends on the velocity

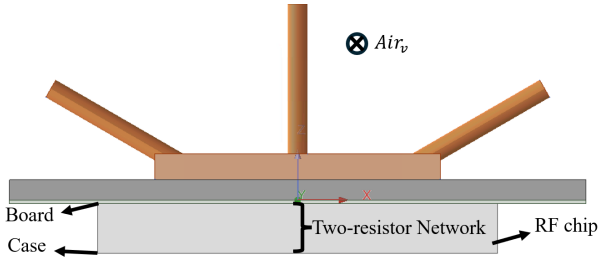


Figure 4: ICEPAK model of the unit element

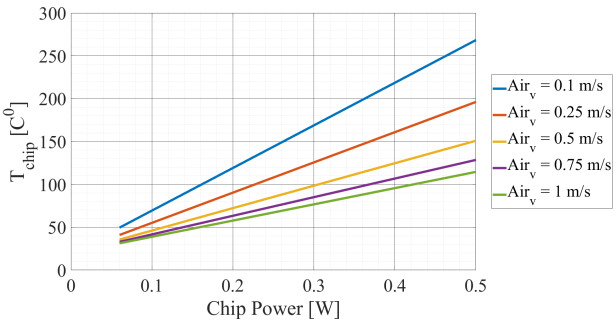


Figure 5: T_{chip} values of unit element with different chip power and air speed values.

of the forced air and the power generated by the chip. The temperature increases with the increase of the generated power and reduces with the increase in the air speed, as expected. The chip temperature (T_{chip}) derived from different chip powers and air speeds can be seen in Fig. 5. In the rest of the study, our RF power will be taken as 0.25 W per antenna element. The cooling challenge is more pronounced in the low-speed air flow due to reduced convection. This study will focus on an air speed of 0.5 m s^{-1} to deal with the slow air flow conditions. The standard patch antenna has 95.4 °C chip temperature in the simulation environment defined above. The HS antenna element with flared fins reduces the chip temperature to 85.4 °C by cooling it down by 10 °C.

3. EM Issues in the Heatsink Antenna Arrays and Proposed Dual-Functional Solutions

The next step of the study deals with the arraying of the heatsink antenna element and introducing dual-functional solutions to the problems associated with the array structure. The beam steering capability of the array is desired to be ±45° in the array plane; therefore, an 8-element linear array will be studied.

3.1. Reduction of Mutual Coupling

One of the major problems in the dense HS array with $\lambda/2$ inter-element spacing is mutual coupling between the elements. Mutual coupling needs to be decreased as it reduces the maximum radiated power and the realized gain of the array. The isometric view of the HS antenna array and the element numbering can be seen in Fig. 6.

The isolation between neighbouring elements is simulated as −13.17 dB for a conventional patch array with $\lambda/2$ interelement distance. The isolation values are observed to be worse

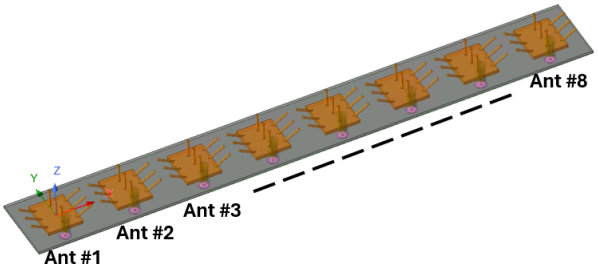


Figure 6: Isometric view of the heatsink antenna array.

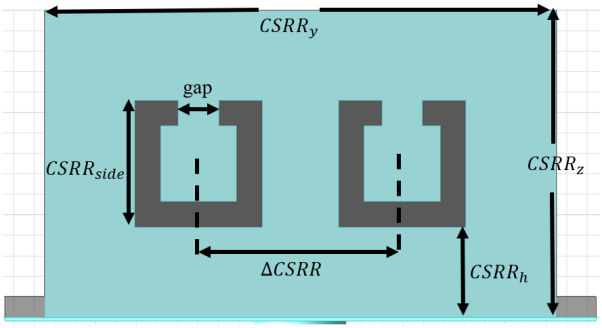


Figure 7: Front view and the dimensions of the CSRR wall.

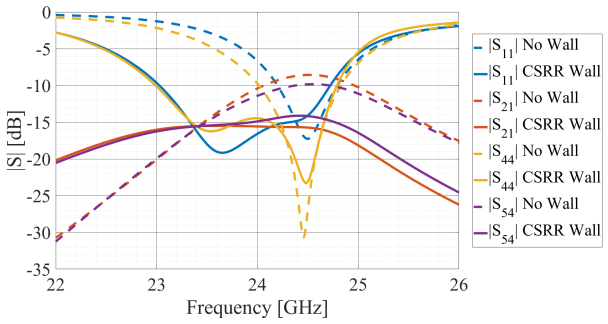


Figure 8: $|S_{11}|, |S_{21}|, |S_{44}|, |S_{54}|$ parameters of the array with (solid) and withouth (dashed) CSRR walls.

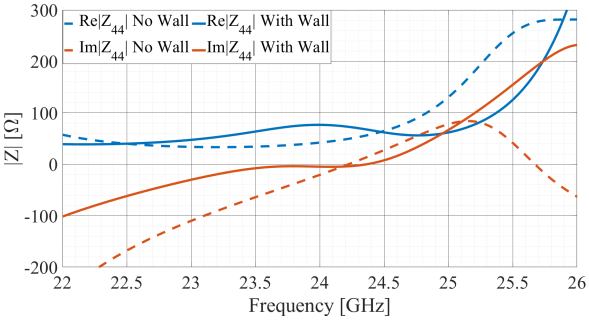


Figure 9: Real and imaginary parts of the Z_{44} for regular array (dashed lines) and array with CSRR walls (solid lines).

for the HS patch array due to additional coupling mechanisms of the fins. The coupling between edge elements in the HS patch array is simulated as $|S_{21}| = -8.56\,\text{dB}$ while the coupling between middle elements is $|S_{54}| = -9.8\,\text{dB}$. The coupling values between elements are too high to secure reliable operation and beam scanning. To increase the isolation a Complementary Split Ring Resonators (CSRR) will be introduced between unit elements.

In this design antenna element mutual coupling due to radiated fields and surface waves needs to be suppressed. A grounding wall between elements is introduced to prevent surface wave propagation. Coupling through radiation is suppressed by resonating structures between antennas. Split ring type resonators are a good candidate to hold radiated fields and prevent radiation. In this design, we aim for dual functionality, meaning that we improve isolation while reducing chip temperature. CSRR structure is preferred to achieve dual functionality by introducing new convection surfaces to the array. Front view of the CSRR wall and its dimensions can be found in Fig.7, and Table. 2.

Improvement in the isolation can be seen by investigating reflection coefficients. The impedance matching, bandwidth, and isolation values can be observed by $|S_{11}|, |S_{21}|, |S_{44}|, |S_{54}|$ parameters from Fig. 8. In this figure, dashed lines represent arrays without CSRR walls, and solid lines represent those with

Table 2: Dimensions of the CSRR wall

Variable	Dimension	Variable	Dimension
$CSRR_y$	5 mm	$CSRR_{side}$	1.24 mm
$CSRR_z$	3 mm	$\Delta CSRR$	2 mm
$CSRR_h$	1.25 mm	gap	0.395 mm

CSRR walls. The isolation value is improved for both center and edge elements to $-15\,\text{dB}$ while the impedance band is broadened.

3.2. Bandwidth Enhancement

The CSRR structures are mainly a solution to the mutual coupling problem; however, they can be assigned to additional functionalities. In this subsection, we will investigate the effects of the CSRR wall on the impedance behaviour and, therefore, the bandwidth of the antenna. The CSRR walls are primarily used for reducing the mutual coupling. Therefore, the optimization of the dimensions is done to maximize the antenna elements isolation. Bandwidth enhancement is done by arranging the feed point of the antenna after determining the CSRR wall dimensions. The HS antenna is a resonant type antenna, so we expect its $Re(Z)$ to become $50\,\Omega$ and have a very small $Im(Z)$ for a narrow frequency bandwidth, which is what we get for the array without the CSRR wall. As the side fins of the HS antenna are very close to the CSRR wall, a surface current is induced. This induced current acts as a top loading to the fins and allows additional current paths, which are longer than the no-wall case. This loading effect makes $Im(Z)$ closer to zero for an extended frequency range. Impedance extension occurs towards lower frequencies due to an extra current path on the fins. Real and imaginary parts of the Z-parameter of the middle element can be seen in Fig.9 for a regular array and an array with CSRR walls. The impedance bandwidth of the antenna is increased from 3.33 % to 7.5 % thanks to the CSRR walls.

4. EM-Thermal Simulation Results of the 8-Element Array

The HS array with CSRR wall outperforms its standard no-HS counterpart in terms of footpring, impedance and mutual coupling characteristics as mentioned, and the design is finalized accordingly. The isometric view of the 8-element design can be seen in Fig.10. However, the radiation characteristics, radiation bandwidth, and efficiency metrics need further investigation. In addition to these EM related parameters, the cooling mechanisms and resulting chip temperatures should be investigated on an array scale. The EM and thermal performance analysis of the array can be found in the following sections.

4.1. Electromagnetic Results

To determine the operational band of the antenna, the radiation characteristics through the impedance bandwidth should be investigated. The array is matched between 22.8 GHz and 24.8 GHz. The realized gain of the array between these frequencies can be seen in Fig.11 for the broadside and $\theta = 45°$ scan. The matching of the antenna can also be observed form active reflection coefficients ($|S^{act}|$). The $|S^{act}|$ values for array with CSRR walls can be seen in Fig. 12. In this figure blue curves represent $|S^{act}_{11}|$ while the orange curve illustrates $|S^{act}_{44}|$ with different scan directions.

The impedance bandwidth of the antenna indicates the ratio of the accepted power by the antenna; however, it is not enough to determine if the accepted power is radiated as desired or not. The radiation pattern bandwidth of the array needs to be checked. The radiation bandwidth can be examined by the total efficiency of the antenna in Fig.13. In this paper the efficiency higher than 60 % will be accepted as a proper radiation as the gain difference within this region would be less than 2.2 dB. The radiation bandwidth of the antenna can be taken between 22.15 GHz and 25.15 GHz (12.7 %) for broadband beam. The radiation bandwidths of the scan angles of $\theta = 30°$ and $\theta = 45°$ are 12.5 % and 10.75 %. The improvement in the bandwidth is exceptional compared with the bandwidth of the 8-element rectangular patch antenna, which is only 2 % (between 24 GHz and 24.5 GHz). The HS antenna element and CSRR walls increased the operational band by 6 times compared to the conventional design. Detailed analysis of the directivity, gain, and realized gain can be seen in Table. 3.

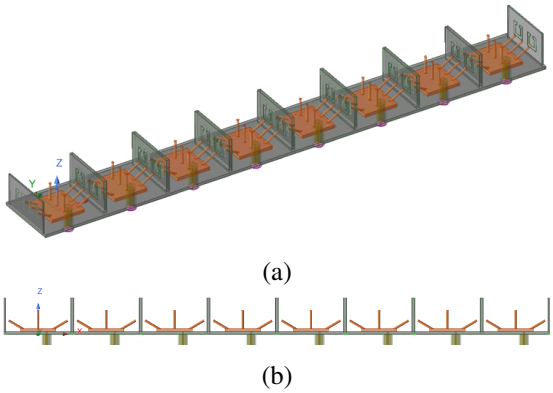


Figure 10: Isometric(a), and side (b) view of the 8 element array with CSRR walls.

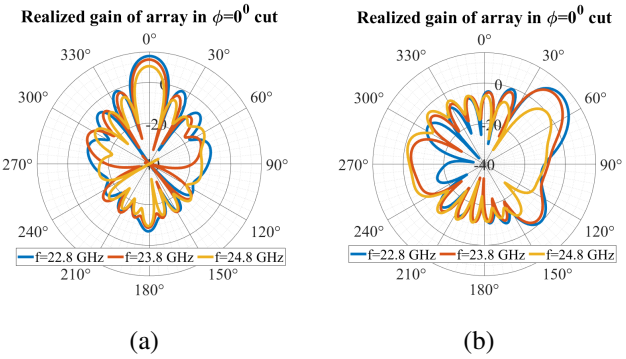


Figure 11: Realized gain values of the array at 22.8 GHz, 23.8 GHz, and 24.8 GHz in: (a) broadside, and (b) $\theta = 45^o$ scan.

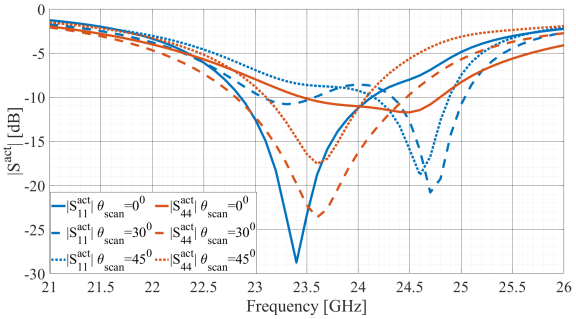


Figure 12: $|S^{act}_{11}|$ and $|S^{act}_{44}|$ parameters of the array with CSRR walls for scan directions $\theta = 0^0, 30^0$, and 45^0.

4.2. Thermal Results

Thermal analysis of the array is performed similarly to the unit element. CFD simulations are realized in the ANSYS ICEPAK environment for different forced air speeds. The air is assumed to flow in the y-direction with speeds 0.1,0.5, and 1 m/s. Two different RF chip structures are considered. The first chip structure supports four RF channels; therefore, two of these chips are needed to feed an 8-element array. These chips are located board side of the dielectric between antenna elements 2-3 and elements 6-7 as numbered in Fig. 6. The assumption of 0.25 W power per antenna is used, so each chip

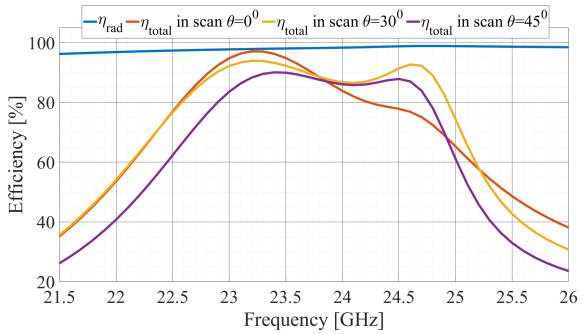
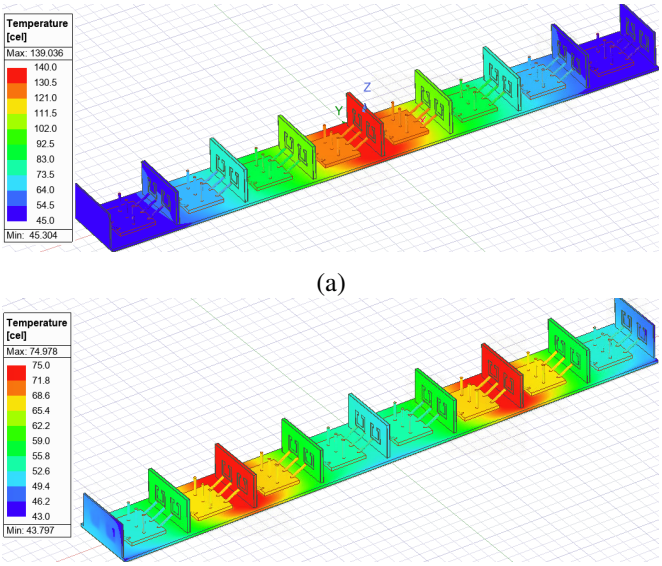


Figure 13: Radiation and total efficiency of the array with CSRR walls for scan angles $\theta = 0^o$,$\theta = 30^o$,and $\theta = 45^o$.

Table 3: Directivity, Gain and Realized Gain values of the HS array with CSRR wall through impedance bandwidth in different scan directions.

	Frequency [GHz]	21.6	22	22.4	22.8	23.2	23.6	24	24.4	24.8	25.2	25.6
Scan $\theta = 0^0$	Directivity [dB]	13.15	13.25	13.35	13.43	13.5	13.47	13.26	12.55	12.05	12.55	13
	Gain [dB]	12.99	13.1	13.22	13.32	13.4	13.4	13.2	12.5	12	12.5	12.94
	Realized Gain [dB]	9	10.54	11.93	12.94	13.36	13.15	12.5	11.49	10.64	10.18	9.64
Scan $\theta = 30^0$	Directivity [dB]	12.36	12.36	12.32	12.22	12	11.47	10.48	10.14	10.5	10.91	12.05
	Gain [dB]	12.2	12.23	12.2	12.12	11.9	11.39	10.38	10.01	10.3	10.7	11.87
	Realized Gain [dB]	8.25	9.7	10.9	11.65	11.72	11.07	9.86	9.66	9.99	8.56	8.01
Scan $\theta = 45^0$	Directivity [dB]	12.44	12.47	12.43	12.3	12.01	11.35	10.01	9.28	9.08	9.1	11.35
	Gain [dB]	12.24	12.3	12.28	12.17	11.88	11.23	9.86	9.07	8.75	8.73	11.02
	Realized Gain [dB]	7	8.57	10.04	11.12	11.47	10.86	9.35	8.69	8	5.74	6.16



(a)

(b)

Figure 14: Surface temperature distribution of the one-chip excitation (a) and two-chip excitation (b) scenarios.

is driven with 1W of power. On the other hand, the second chip structure assumes eight-channel excitation. One chip located in the middle of the array with 2 W power is sufficient to get the same excitation as the first chip. Locations of the chips in both first and second scenarios are selected to be as symmetric as possible to ease the microstrip connections to the antennas.

Table 4: Chip temperatures of the Patch and HS patch array with CSRR walls for one and two chip scenarios

	Air_v	0.1 m/s	0.5 m/s	1 m/s
Conv. Patch Array	Two Chips (1W each)	182.84^0C	97.3^0C	73.3^0C
	One chip (2W)	264.46^0C	171.7^0C	143.32^0C
Heatsink Patch Array	Two Chips (1W each)	143.84^0C	70.3^0C	51.86^0C
	One Chip (2W)	222.7^0C	138.9^0C	114.3^0C

The temperature values recorded in each case can be seen in Table. 4. The thermal simulation results illustrate that using multiple RF chips by placing them in a distributed manner reduces the chip temperature. The chip temperature drops from 138.9 °C to 70.3 °C when the total RF power is maintained but divided equally and distributed across two distinct locations. The surface temperature distribution of the single source and two source cases can be seen in Fig. 14.

5. Conclusions

This study introduces an innovative heatsink-antenna array concept that effectively merges thermal management and electromagnetic performance in a single, integrated structure. By employing tilted fin heatsinks on top of patch antennas, the design achieves antenna miniaturization of 8 % compared to conventional rectangular patch and a major reduction in chip temperature from 95.42 °C to 85.41 °C for the single element. Further, the integration of CSRR-based isolation walls between elements significantly reduces mutual coupling and broadens the impedance bandwidth. Comprehensive EM and thermal simulations validate the performance gains, demonstrating a radiation bandwidth increase to 12.7 % compared to 2 % bandwidth of the conventional patch array and a substantial reduction in chip operating temperatures from 97.3 °C to 70.3 °C, especially in low airspeed environments like 0.5 $m\,s^{-1}$ airflow. The array design not only enables efficient beam steering and low cross-polarization around −45 dB but also offers scalable thermal benefits through distributed chip placement. The maximum temperature of the chip can be reduced from 171.7 °C to 138.9 °C by using two separately located chips instead of one chip. These findings underscore the potential of dual-purpose heatsink antennas as a viable solution for next-generation high-density and high-power antenna systems, particularly in 5G, radar, and mm-wave communication applications.

Acknowledgment

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